A SYSTEM AND METHOD OF HEAT DISSIPATION IN SEMICONDUCTOR DEVICES

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A SYSTEM AND METHOD OF HEAT DISSIPATION IN SEMICONDUCTOR DEVICES

BACKGROUND

[0001] This disclosure relates to the design and fabrication of semiconductor devices, and more specifically, to a system and method of heat dissipation for semiconductor devices.

[0002] Heat generation from electronic devices is well known. For example, a typical microprocessor typically consumes approximately 40 watts of electricity, a majority of which will eventually be transformed into heat. However, if the heat is not well dissipated, the performance of electronic devices may be degraded--poor heat dissipation may cause damages to electronic devices, and reduce the reliability and life expectancy of the devices.

[0003] Generally, heat produced in a semiconductor device is dissipated by device conduction. Typically, heat simply emits through materials utilized to form the basic wiring structure of the semiconductor device. Frequently, no special structures are provided to help dissipate heat within the semiconductor device.

[0004] Prompted by the advancement of integrated circuit materials and design, new generations of semiconductor devices possess smaller and more complex circuits, thereby enhancing the need for heat dissipation. In addition, low-k materials have been introduced to replace the conventional SiO2 material to address RC delay issues. However, most of the low-k materials possess poor thermal conductivity.

[0005] Accordingly, it is desired to provide an improved system and method for dissipating heat in semiconductor devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Fig. 1 illustrates a cross-sectional view of a semiconductor substrate with a first level metallurgy according to one embodiment of the present disclosure.

[0007] Fig. 2 illustrates a cross-sectional view of a semiconductor substrate with a first level metallurgy that includes a dummy structure according to one embodiment of the present disclosure.

[0008] Fig. 3 illustrates another cross-sectional view of a semiconductor substrate with a first level metallurgy that includes dummy structures according to one embodiment of the present disclosure.

[0009] Fig. 4 illustrates a top view of a semiconductor metallurgy layer that includes dummy structures according to one embodiment of the present disclosure.

[0010] Fig. 5 illustrates a top view of a metallurgy layer that includes connected dummy structures according to one embodiment of the present disclosure.

[0011] Fig. 6 illustrates a top view of a metallurgy layer that includes dummy structures that are connected to vias according to one embodiment of the present disclosure.

[0012] Fig. 7A-7D illustrates cross-sectional views of a partial semiconductor device according to one embodiment of the present disclosure.

DETAILED DESCRIPTION

[0013] This disclosure relates to semiconductor devices and the design and fabrication thereof, and more specifically, to a system and method of heat dissipation for semiconductor devices.

[0014] For the purposes of promoting an understanding of the principles of the disclosure, references will now be made to the embodiments, or examples, illustrated in the drawings and specific languages will be used to describe the same. It will nevertheless be understood that no limitation of the scope of the disclosure is thereby intended. Any alterations and further modifications in the described embodiments, and any further applications of the principles of the disclosure as described herein are contemplated as would normally occur to one skilled in the art to which the disclosure relates.

[0015] Referring now to Fig. 1, shown therein is a cross-sectional view of a partial semiconductor device according to one embodiment of the present disclosure. In this embodiment, a substrate 10 may comprise a field effect transistor, which includes source and drain regions 12 and a gate 14. The substrate 10 may also comprise a field oxide layer 16, and a relatively thick borophosphosilicate glass (BPSG) layer 18. Alternate embodiments may include a shallow trench isolation or a split gate. While the drawings show the N+ source and drain regions 12, it is understood by those skilled in the art that the conductivity types may be different. In this example, a first metallurgy level may reside on the surface of the substrate 10, and may comprise metal lines 20 (one or more operative conductive lines that are closely spaced), and a more distantly spaced operative conductive metal line 22. To properly construct the conductive lines 20 and 22, design rules are utilized for the particular application to specify the necessary widths of the conductive lines and the distances between them. In one example, the width of a conductive line may be approximately equal to the distance between the conductive lines. Also, the feature size, which may be defined by a number of factors, such as the wavelength of the light used to expose the pattern, the type of resist, and other factors that are known in the art, may restrict the minimum dimensions of the conductive lines.

[0016] Referring now to Fig. 2, shown therein is another partial semiconductor device that includes a dummy structure 42 that may help dissipate heat according to one embodiment of the present disclosure. In this embodiment, the conductive line pattern (e.g., lines 20, 22) may be examined to locate vacant areas for positioning dummy structures. In one example, when the distance between conductive lines equals to or exceeds three times the width of the conductive line, a dummy structure may be positioned in the vacant space. However, dummy structures may also be placed when the distance between the conductive lines is smaller. The placement of dummy structures may take into consideration the possible capacitance that may be generated between the conductive lines and the dummy structures. To prevent the generation of significant capacitance, it may be advisable to maintain a distance of at least 0.1 micrometer between a dummy structure and a conductive line. However, it is contemplated that a shorter distance is also possible, as long as the dummy structure is separate from the conductive line. It is contemplated that the sizes of the dummy structures may be flexible.

[0017] Referring now to Fig. 3, shown therein is another partial semiconductor device that includes a plurality of dummy structures 44 that help to dissipate heat according to one

embodiment of the present disclosure. In this embodiment, a plurality of dummy structures may be placed when the distance between the conductive lines is smaller than five times the widths of the conductive lines, or if the width of the dummy structure is smaller than three times the widths of the conductive lines. However, a plurality of dummy structures are also contemplated under other distances and widths. In addition, the distances between and among the dummy structures may be varied over a wide variety of ranges. Therefore, a variety of flexibility is anticipated in positioning the dummy structures.

[0018] In furtherance of the example, each of the structures 44 may comprise a rectangular prism, polygon, partial rectangular prism, cube, partial cube, sphere, partial sphere, pyramid, partial pyramid, cone, partial cone or other regular or irregular shapes. It is contemplated that each of the structures 44 may comprise copper, aluminum, other type of metals, or other materials suitable for heat dissipation. It is also contemplated that all of the structures 44 may comprise the same type of metal. Alternatively, at least two of the structures 44 may comprise different types of metals. Further, it is contemplated that each of the structures 44 may comprise a variety of sizes. In one example, the structures 44 may comprise a height similar to those of the conductive lines. However, other heights of the structures 44 are also contemplated.

[0019] Referring now to Fig. 4, shown therein is a top view of a metallurgy layer that includes a plurality of dummy structures 50 for heat dissipation according to one embodiment of the present disclosure. In this embodiment, the widths of the dummy structures may be less then one micrometer to prevent possible hillock growth, which could cause potential shorting between metallurgy levels. In addition, widths of the plurality of dummy structures 50 may be similar to produce a more smooth etching or patterning of the conductive lines and the dummy structures. However, it is also contemplated that the widths of the dummy structures 50 may be at least one micrometer, and that the widths of the plurality of dummy structures 50 may differ. In one example, the distance d1 between two dummy structures is equal to the distance d2 between another two dummy structures. Similarly, d3 may be equal to d1. However, it is also contemplated that distances between dummy structures may differ.

[0020] Referring now to Fig. 5, shown therein is another top view of a metallurgy layer that includes a plurality of dummy structures 50 according to one embodiment of the present disclosure. In this embodiment, dummy structures 50A and 50B are connected by a line 52, and dummy structures 50B and 50C are connected by a line 54. Likewise, other dummy structures

are also connected by various lines. It is contemplated that each of the lines 52 and 54 may comprise copper, aluminum, other types of metals, or other materials suitable for heat dissipation. It is also contemplated that the line 52 and the dummy structure 50B may comprise the same type of material, or that they may comprise different materials.

[0021] In furtherance of this example, the width of the line 52 or 54 may be smaller than that of the dummy structure 50A. However, it is also contemplated that the width of the line 52 or 54 may be equal to or larger than that of the dummy structure 50A. Further, each of the lines 52 and 54 may comprise a rectangular prism, polygon, partial rectangular prism, cube, partial cube, sphere, partial sphere, pyramid, partial pyramid, cone, partial cone or other regular or irregular shapes.

[0022] Referring now to Fig. 6, shown therein is another top view of a simplified metallurgy layer 80 of a semiconductor device according to one embodiment of the present disclosure. In this embodiment, dummy structures 56, 58 and 60 are connected together by lines 62 and 64. In fact, all the dummy structures located on side A of a conductive line 72 have been connected together. Likewise, all the dummy structures located on side B of a conductive line 72 have been connected together. Here, one or more lines 66 are utilized to connected dummy structures on side A of the conductive line 72 to a seal ring 68. Likewise, one or more lines 74 are utilized to connected dummy structures on side B of the conductive line 72 to the seal ring 68. Through one or more vias 70, the seal ring 68 of the metallurgy layer 80 may be connected to the seal rings of other metallurgy layers. Accordingly, dummy structures on the metallurgy layer 80 may be connected to dummy structures on other metallurgy layers. It is contemplated that not all dummy structures on side A or B of the conductive line 72 may be connected. As a result, not all dummy structures on the metallurgy layer 80 may be connected to dummy structures on other metallurgy layers. Further, each of the lines 66 and 74 may comprise a variety of shapes, materials and sizes. For example, each of them may comprise a rectangular prism, polygon, partial rectangular prism, cube, partial cube, sphere, partial sphere, pyramid, partial pyramid, cone, partial cone or other regular or irregular shapes. It is contemplated that each of the lines 66 and 74 may comprise copper, aluminum, other type of metals, or other materials suitable for heat dissipation. Further, the widths of the lines 66 and 74 may be larger than one micrometer. Alternatively, the widths of the lines 66 and 74 may be no more than one micrometer. Finally, each of the lines 66 and 74 may be identical or different.

[0023] Referring now to Fig. 7A, shown therein is a cross-sectional view of a partial semiconductor device according to one embodiment of the present disclosure. In this embodiment, a dielectric layer 86 may be formed over lines 20, 22, and 42 to level topology. In one example, the layer 86 may be formed by plasma enhanced oxidation (PE-OX), with a thickness in the range of about 400 to 3000 Angstroms. The layer 86 may be deposited by plasma enhanced chemical vacuum deposition. It is contemplated that the layer 86 may comprise other thickness parameters and deposition methods.

[0024] Referring now to Fig. 7B, shown therein is another cross-sectional view of a partial semiconductor device according to one embodiment of the present disclosure. In this embodiment, a dielectric layer 88 may be deposited by spin-on-glass techniques (SOG) and cured. The layer 88 may be used to fill in the gaps between the lines and, therefore, presents a relatively planar surface. The layer 88 may be deposited by spin-on-glass techniques, baked at between about 150 to 260 centigrade degrees for a few minutes to remove the solvents from the layer, and cured at between about 400 to 450 centigrade degrees for 30 to 60 minutes to form the silicon oxide insulating layer.

[0025] Referring now to Fig. 7C, shown therein is another cross-sectional view of a partial semiconductor device according to one embodiment of the present disclosure. In this embodiment, the top surface of the dielectric layer 86 and 88 may be etched back after spin-on-glass curing to further enhance the surface planarity. The procedure may be achieved by anisotropic reactive ion etching processes.

[0026] Referring now to Fig. 7D, shown therein is another cross-sectional view of a partial semiconductor device according to one embodiment of the present disclosure. In this embodiment, a top dielectric layer 90 may be deposited by plasma enhanced chemical vapor deposition (PE-CVD) techniques. The layer 90 may have a thickness of approximately 2000 to 8000 Angstroms. Vias may then be formed in the dielectric layers 86 and 88, and another metallurgy level and dielectric layer may be formed according to procedures known in the art.

[0027] Many variations of the above disclosure are also contemplated by the present disclosure. In one example, instead of constructing a plurality of dummy structures on a metallurgy layer and connecting them, one large metal structure may be utilized. In another example, dummy structures from one metallurgy layer may be selectively connected to one or more other metallurgy layers. In a third example, some dummy structures on a given metallurgy

layer may not be connected. In a fourth example, some dummy structures on a given metallurgy layer may not be connected with dummy structure(s) of other metallurgy layers. In addition, dummy structures are also described in the U.S. Patent No. 5,905,289 entitled "Process for Producing a Semiconductor Device with a Planar Top Surface" to Lee, which is hereby incorporated by reference in its entirety.

[0028] Although only a few exemplary embodiments of this disclosure have been described in detail above, those skilled in the art will readily appreciate that many modifications are possible in the exemplary embodiments without materially departing from the novel teachings and advantages of this disclosure. Also, features illustrated and discussed above with respect to some embodiments can be combined with features illustrated and discussed above with respect to other embodiments. Accordingly, all such modifications are intended to be included within the scope of this disclosure.